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DESIGN OF A THREE-PHASE,
15-KILOVOLT-AMPERE STATIC INVERTER
FOR MOTOR-STARTING A BRAYTON
SPACE POWER SYSTEM

by Robert J. Frye and Arthur G. Birchenough

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Cleveland, Ohio 44135

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16. Abstract The design of a three-phase, 400-Hz, 15-kVA static inverter for motor-starting the 2- to 15-kWe Brayton electrical space power system is described. The inverter operates from a nominal 56-V dc source to provide a 28-V, rms, quasi-square-wave output. The inverter is capable of supplying a 200-A peak current. Integrated circuitry is used to generate the three-phase, 400-Hz reference signals. Performance data for a drive stage that improves switching speed and provides efficient operation over a range of output current and drive supply voltage are presented. A transformerless, transistor output stage is used.					
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DESIGN OF A THREE-PHASE, 15-KILOVOLT-AMPERE STATIC INVERTER FOR MOTOR-STARTING A BRAYTON SPACE POWER SYSTEM

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SUMMARY

The design of a three-phase, 400-hertz, 15-kilovolt-ampere, prototype static inverter is discussed. The inverter is designed to start the 2- to 15-kilowatt isotope Brayton power system by providing the power necessary to operate the alternator as a motor. For this application, the inverter must supply a high current for a short period of time. The inverter operates from a nominal 56-volt dc source. The output is a three-phase quasi-square wave, approximately 28 volts rms.

The major features of the inverter design are (1) a simple reliable oscillator stage using an integrated-circuit operational amplifier to provide the 1200-hertz reference signal; (2) an all-integrated-circuit digital logic stage for generating the three-phase, 400-hertz reference signals; (3) a unique drive circuit for the output-stage transistors that increases switching speed, reduces power loss, and provides the necessary drive current over a range of drive supply voltages; and (4) a transformerless output stage.

Data showing the performance of the drive stage are presented, as well as a typical Brayton system startup using the inverter. The inverter has been successfully used for 50 Brayton system startups.

INTRODUCTION

The Lewis Research Center is currently testing a Brayton cycle system for electrical power generation in space. This system consists of a heat source, a power conversion system, and a heat rejection loop. The system is designed to produce a 2- to 15-kilowatt electric output from either a radioisotope or solar heat source. This closed-loop system uses a mixture of helium and xenon as the working gas. In the power conversion system, a single-shaft assembly supported by gas bearings and consisting of a turbine, alternator, and compressor operates at a design speed of 36 000 rpm (377 rad/

sec) to supply the 1200-hertz electrical power. (Ref. 1 further describes the system.)

Brayton electrical power systems require a subsystem to start rotation of the turbine-alternator-compressor. Startup of this system has been accomplished by two methods. These methods are (1) injecting gas into the system from a high-pressure storage tank (ref. 2), and (2) operating the alternator as a motor from an auxiliary power source. This latter method of startup has the advantage of conserving gas in the system and eliminates the values required for injection startup. Conserving gas in the system is very important if restart capability of the system is required.

The feasibility of motor-starting the Brayton system was investigated by first determining the motoring characteristics of the alternator (ref. 3). Then system startups with the motoring technique were performed by using a three-phase, variable voltage and frequency, sine-wave power source (refs. 4 and 5). This testing indicated that a 400-hertz motoring frequency provided self-sustaining operation of the system. Also, when operating at this frequency, a 20-volt ac, rms, alternator line-to-neutral voltage provided sufficient torque to start the system. Further results of this testing indicated that motoring performance was relatively insensitive to small changes in voltage or frequency. Based on the success of these tests, a solid-state inverter was designed and fabricated. The inverter, which receives its power from the system battery source, provides the necessary ac power to operate the alternator as a motor.

The major requirement of the inverter is the ability to supply a large peak starting current for a short period of time. The remainder of the inverter operation is a lower power motoring condition at near synchronous speed. The inverter was designed to produce a 400-hertz output, as a result of the system testing previously mentioned. Since a 20-volt rms, line-to-neutral voltage was required at this frequency, and since small changes in voltage were not critical to motoring performance, the inverter was designed to operate directly from the system, 56-volt, unregulated battery supply. To further simplify inverter design, a quasi-square-wave inverter output was chosen. Thus, the inverter was designed to produce a 15-kilovolt-ampere, three-phase, 400-hertz, quasi-square-wave output from a nominal 56-volt dc source. The output voltage is approximately 28 volts rms, while the peak current rating is 200 amperes per phase. The inverter is packaged as a prototype flight unit and will be used in an environmental simulation test of the Isotope Brayton system.

The prototype flight version of the inverter is shown in figure 1. For this inverter design, integrated circuits are used to generate the three-phase, 400-hertz reference signals. Also, a drive circuit was designed that minimized drive power loss, increased output transistor switching speeds, and eliminated the need for a drive voltage supply regulator. A pulsed on-off control circuit is provided to interface with the Brayton system controls. An input contactor is included in the design to isolate the inverter from the dc source.

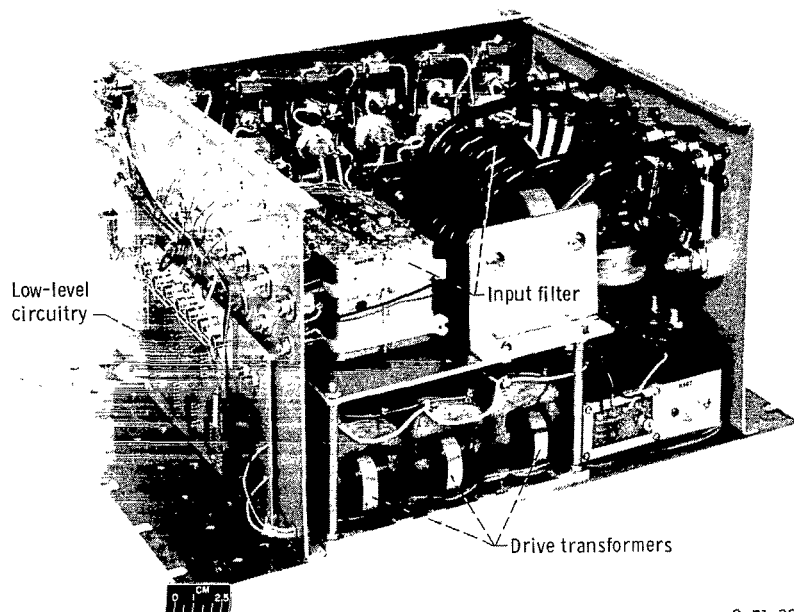


Figure 1. - Motor-start inverter.

This report describes the inverter circuitry, presents data showing drive-stage circuitry performance, and shows how the inverter is used in a typical Brayton system startup.

INVERTER CIRCUIT DESCRIPTION

A block diagram of the inverter is shown in figure 2. The input power for the inverter is supplied by a nominal 56-volt dc source. The three-phase output of the inverter is connected to the alternator. The inverter block diagram is divided into two sections, the low-level circuitry and the power circuitry. The low-level circuitry includes the low-voltage regulator, the circuitry that is supplied by the regulator, and the pre-drive stage. The power circuitry includes the drive stage, the output stage, and the input filter. The inverter has a three-phase, 28-volt, rms, quasi-square-wave output.

The inverter circuitry functions in the following manner: A 1200-hertz square-wave signal is generated by the oscillator. This signal is fed to the three-phase divider circuitry, where it is converted into three 400-hertz, square-wave signals displaced by 120° . These three signals and their complements (logical inversions) are fed to the dwell-time stage. The dwell-time stage delays the leading edge of each of the six three-phase divider signals to prevent conduction overlap of the output-stage transistors. The predrive stage provides the current amplification required for the drive stage.

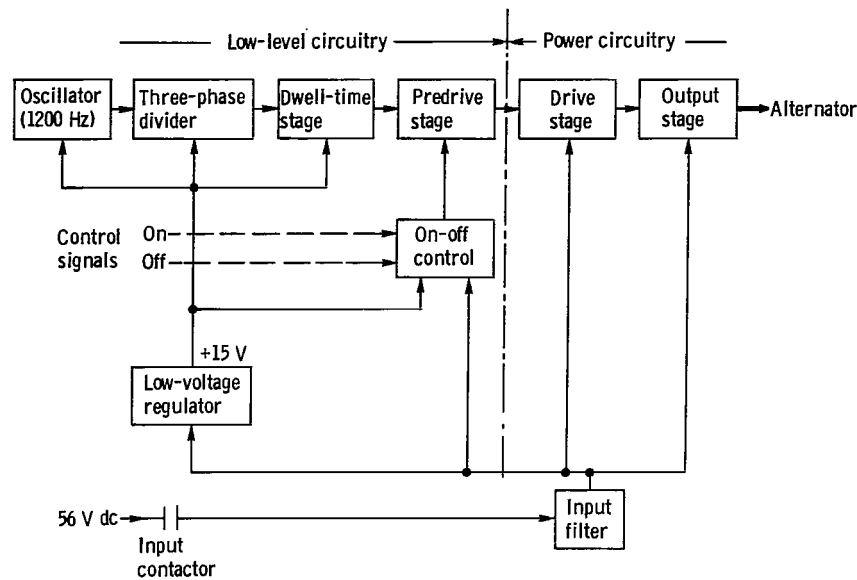


Figure 2. - Block diagram of inverter circuitry.

The on-off control provides an electronic means of turning the inverter on and off by switching the supply voltage to the predrive stage. Thus, in the off mode, drive signals will be present only up to the predrive circuitry. An input contactor is used on the 56-volt input to the inverter to completely isolate the inverter from the dc source. The low-voltage regulator provides 15 volts dc to the low-level circuitry.

The six predrive signals are further amplified by the drive circuitry to become the base drive signals for the three half-bridge transistor circuits of the output stage. The load, in this case the alternator, is connected to the output stage through an external contactor. An input filter is necessary to attenuate third harmonic current. A complete inverter schematic circuit diagram is presented in the appendix. The circuits identified in the block diagram of the inverter are discussed in the following sections.

Low-Level Circuitry

The low-level circuitry makes extensive use of linear and digital integrated circuits. The integrated-circuit logic family selected exhibited a high degree of inherent noise immunity, a high input threshold, and a large logic swing. This logic has a minimum 5-volt noise margin and operates from a 15-volt dc supply. These logic characteristics provide excellent electrical noise immunity and allow easy interfacing with other components.

Oscillator. - The first stage of the low-level circuitry is the oscillator. The oscillator provides a 1200-hertz square-wave signal with an output voltage swing of approximately

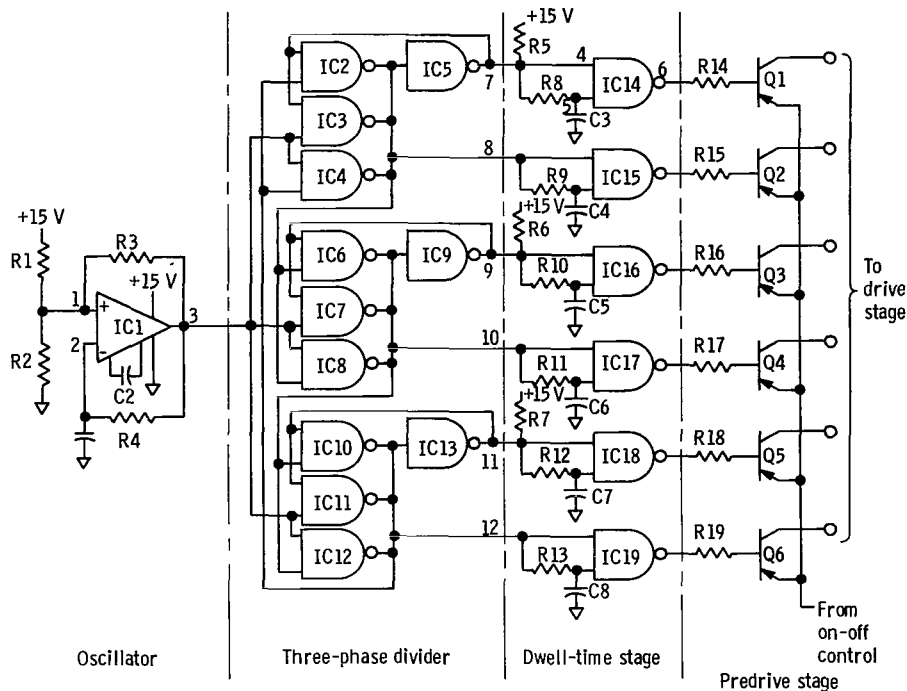


Figure 3. - Low-level logic.

0 to 15 volts. The oscillator circuitry consists of an integrated-circuit operational amplifier, IC1, and the associated components shown in figure 3. Since a single power supply is used for the amplifier, equal value resistors, R1 and R2, are used to provide a bias voltage at the positive input of the amplifier equal to one-half of the supply voltage. R1 or R2 may be trimmed to compensate for the internal offset voltage of the amplifier. Minimizing the offset voltage improves the symmetry of output waveform of the oscillator. Internal frequency compensation of the amplifier is provided by capacitor C2.

The oscillator circuitry waveforms are presented in figure 4. Resistor R3 provides positive feedback and, in conjunction with resistors R1 and R2, determines the swing of the square-wave voltage about the bias point at the positive input of the amplifier. The charging and discharging of the R-C network, R4 and C1, produces an almost triangular waveform at the negative input of the amplifier. A change of state of the amplifier output occurs when the negative input voltage level exceeds the voltage at the positive input of the amplifier. Thus, the amplifier functions as a comparator, operating in a saturated switching mode, at a frequency determined by the R4-C1 time constant.

Three-phase divider. - The three-phase divider circuitry consists of NAND gates IC2 to IC13 as shown in figure 3. This circuitry generates three 120° displaced square-wave signals (outputs of gates IC5, IC9, and IC13) and the complement of each of these three signals (produced at the "wired-ORing" of the outputs of gates IC2 to IC4,

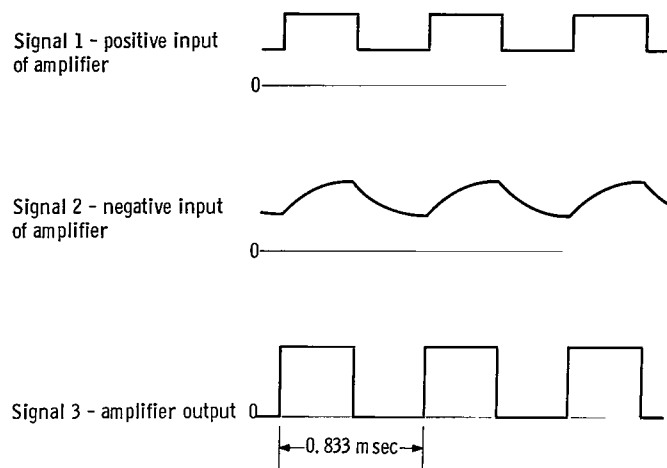


Figure 4. - Oscillator circuitry waveforms.

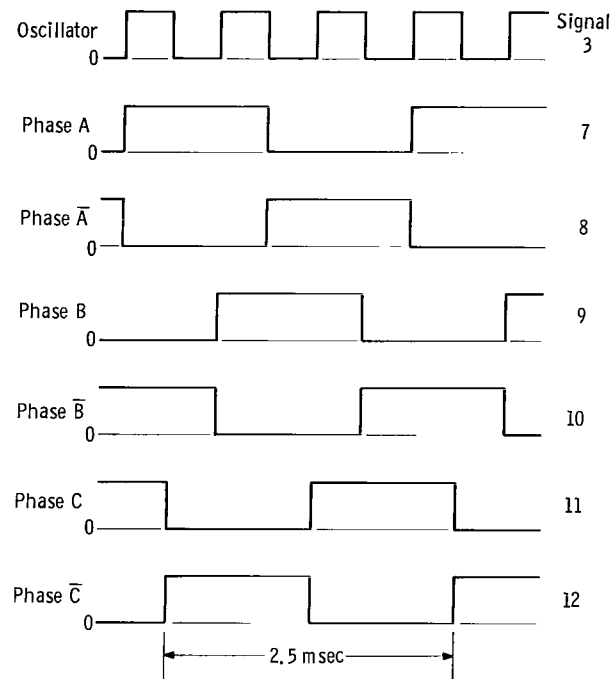
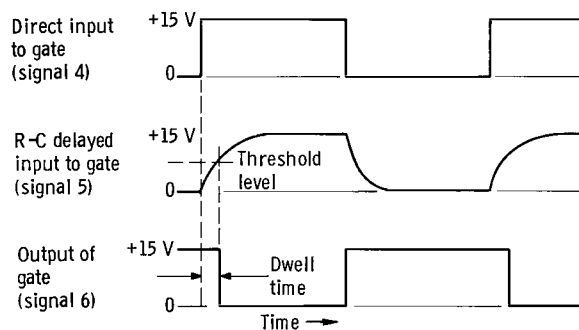


Figure 5. - Timing diagram of oscillator and three-phase divider circuit outputs.

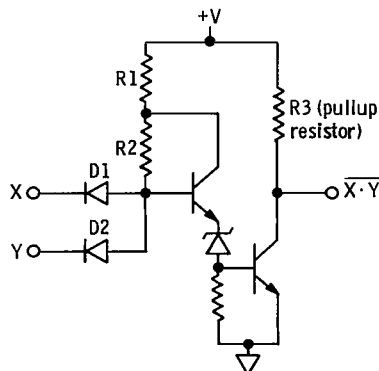
IC6 to IC8, and IC10 to IC12). There is a divide-by-three countdown that occurs in the three-phase divider circuitry. Thus, all the output signals of the three-phase divider circuitry are 400 hertz, the output frequency of the inverter. The conventional methods of obtaining this type of phase shift are through the use of saturable magnetics or L-C delay circuitry. These circuits have the disadvantage that they are sensitive to magnetic core matching and to small changes in supply voltage, frequency, or temperature. The digital circuitry used in the three-phase divider is unaffected by such changes. A timing diagram showing oscillator and three-phase divider circuitry output waveforms is presented in figure 5. The numbers on the right side of figure 5 indicate where the signals appear on the figure 3 schematic. All six three-phase divider output signals are fed to the dwell-time circuitry.

Dwell-time stage. - The purpose of the dwell-time stage is to provide a time delay, or dwell time, between the leading and trailing edges of the complementary outputs of the three-phase divider circuitry. This delay is necessary so that no overlap occurs in the alternate conduction of the transistors in the bridge output stage. Any overlap results in excessively high current spikes through the transistors (ref. 6). The dwell-time circuitry is shown as part of the figure 3 schematic.

Figure 6(a) show the typical inputs and output of a logic gate used in the dwell-time



(a) Timing diagram.



(b) Internal schematic of gate.

Figure 6. - Dwell-time gate.

circuitry. One input to the gate (4 in fig. 3) comes directly from the three-phase divider circuitry. The other input to the gate (5 in fig. 3) is the same as the first but is fed through an R-C delay network (R8 and C3 for IC14). The gate requires two high-level input signals to be enabled. This does not occur until the R-C network voltage reaches the 7.5-volt threshold level of the gate, as shown in figure 6(a). The dwell time is thus determined by the time constant of the R-C network. A dwell-time duration of approximately 100 microseconds was used. The trailing edges of the three-phase divider circuit waveforms are not affected by the dwell-time circuitry, since as soon as the direct input to the dwell-time gate changes state, the gate is no longer enabled and the gate output changes state.

Resistors R5 to R7 are necessary to equalize dwell times by compensating for the effect of the internal "pullup" resistor of each gate (R3 in fig. 6(b)). When gates are "wired-ORed" together, as the outputs of IC2, IC3, and IC4 of figure 3 are, the internal pullup resistors of these gates are paralleled together. But the input of gate IC14 is driven by only one gate, IC5. Therefore, resistor R5 is paralleled with the "pull-up" resistor of IC5. The value of R5 is approximately equal to the parallel combination of two gate pull-up resistors. Likewise, resistors R6 and R7 are added to the inputs of gates IC16 and IC18. Thus, all inputs to the dwell-time circuitry have the same effective resistance to the +15-volt supply. All six dwell-time circuit outputs are fed to the predrive circuitry.

Predrive circuitry. - The predrive stage is a current amplifier for the six dwell-time circuit outputs. The predrive circuitry consists of base-drive-current-limiting resistors R14 to R19 and transistors Q1 to Q6, as shown in figure 3. Unlike the rest of the low-level circuitry, the predrive stage is gated on by the on-off control. The outputs of the predrive stage are fed to the power circuitry portion of the inverter.

On-off control. - This circuitry provides an electronic means of turning the inverter on and off and was designed to interface with the Brayton system controls. A circuit schematic of the on-off control is shown in figure 7. The heart of this circuit is the R-S

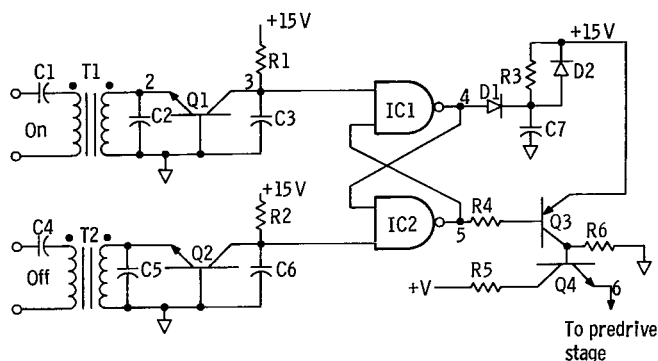


Figure 7. - On-off control circuitry.

(set-reset) flip-flop composed of gates IC1 and IC2. Identical pulse conditioning circuits are used for both "on" and "off" inputs to the flip-flop. The circuitry was designed to operate from a 5-volt pulse of greater than 2-microsecond duration, from a source impedance of 500 ohms or less. The timing diagram in figure 8 illustrates the circuit waveforms for the "on" pulse. Both input pulse circuits function similarly.

The on pulse is applied to transformer T1 through a coupling capacitor, C1. The 2.5:1 ratio transformer, T1, is used to provide electrical isolation, impedance matching, and noise immunity. Capacitors C2 and C3 are both used for noise filtering. Tran-

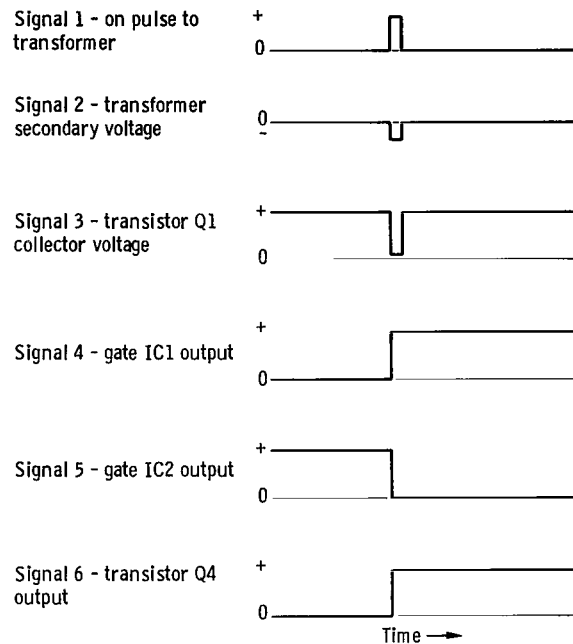


Figure 8. - On-off control timing diagram.

sistor Q1 is used in a common base configuration because voltage gain, not current gain, is needed to convert the signal to a logic level. Thus, an on pulse comes through, is amplified, and sets the flip-flop (as shown in fig. 8). In a like manner, an off pulse will reset the flip-flop. When the flip-flop is set by an on pulse, the output of gate IC2 goes low, causing transistor Q3 to saturate. Transistor Q4, operating in an emitter follower mode, supplies approximately 15 volts. Because on-off control of the inverter is provided at the predrive stage, only a small amount of power is switched. Also, since the remainder of the low-level circuitry is operating, the proper logic sequence has been established and standby power is low.

In order to assure the proper initial state of the R-S flip-flop when dc power is first turned on, diodes D1 and D2, resistor R3, and capacitor C7 are necessary. When the

power is turned on, C7 will start to charge through R3 and the internal resistors of gates IC1 and IC2. The time required for the capacitor to charge to the threshold voltage of a gate must be longer than the rise time of the supply voltage. Thus, the voltage at the output of gate IC1 remains low long enough for the flip-flop to establish its proper state. The diode D1 is necessary to isolate the charged capacitor, C7, from the flip-flop during steady-state operation. Diode D2 is used to allow C7 to discharge quickly when the 15-volt supply is off. Thus, capacitor C7 would be in the discharged state if the power supply were quickly turned back on.

Low-voltage regulator. - The low-voltage regulator schematic is shown in figure 9. This 15-volt regulator is a simple series pass regulator using a zener diode reference, D1. The regulator operates directly off the 56-volt input supply. All the low-level circuitry, except for the predrive stage, is supplied by the low-voltage regulator. Although a more efficient type of regulator, such as a switching regulator, could have been used, the complexity of such a regulator would not be justified considering the operating time of the inverter and the relatively small amount of power (7.25 W, max.) dissipated in the regulator.

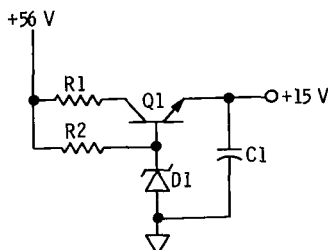


Figure 9. - Low-level voltage regulator.

Power Circuitry

Drive stage. - In the drive stage, shown in figure 10, six identical independent circuits are used to supply base current to each of the six output-stage transistors. By sensing the degree of saturation of an output-stage transistor, the drive circuitry supplies only enough base drive to keep the output transistor collector junction near saturation. Operating the output transistors near saturation results in lower power dissipation due to increased switching speed and higher base drive efficiency over a wide range of output transistor collector currents.

Transistor Q1 (fig. 10) is driven as a saturated switch by the predrive stage. When Q1 is turned on, a positive voltage is induced in the transformer secondary. The induced voltage at pin 6 of the transformer causes a current to flow in R3 and the base of Q2. The

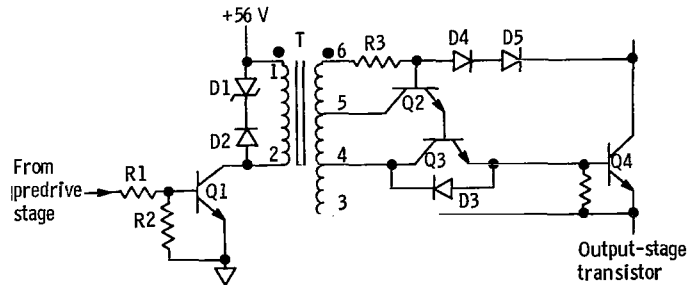


Figure 10. - Drive-stage circuit.

base current of Q2 is amplified by Q2 and Q3 and applied to the base of the output transistor, Q4, turning it on.

Control of the output transistor base current is initiated by sensing the collector voltage of Q4. Whenever the collector voltage of Q4 is lower than its base voltage, current is diverted from the base of Q2 through D4 and D5. The voltage drop across D4 and D5 compensates for the base-emitter voltage drops of Q2 and Q3. The reduction of Q2 base current reduces output transistor Q4 base current. Although increasing the circuit complexity, this method of base drive control reduces the base drive power loss for low-output transistor base or collector currents. Also, the drive circuitry can supply the required base current over a wide drive supply voltage range, eliminating the need for a voltage regulator on the drive supply. The taps on the transformer improve drive circuit efficiency by supplying the proper collector voltages to operate Q2 and Q3 in a nearly saturated mode. When Q1 turns off, the transformer magnetizing current reverses the voltage across the transformer, resetting the core flux and supplying a turn-off pulse to the output transistor through D3.

Actual typical drive circuit waveforms, redrawn from oscilloscope traces, are shown in figure 11. When Q1 turns off, its collector voltage increases to a level determined by D1, D2, and the supply voltage. The drive transformer magnetizing current flows through D1 and D2 until the core resets. The transformer core must have an air gap to avoid becoming saturated. The reverse transformer voltage, coupled through D3, provides a turn-off voltage for the output transistor. Figure 11 also shows typical output transistor collector current for a resistive load and the corresponding Q4 base current supplied by the drive circuit. The base current waveform for Q2 would be approximately the same as for Q4. The current in R3 is essentially constant whenever Q1 is on. The current through D4 and D5 is also shown in figure 11.

The inverter was tested at design conditions using a resistive load. Figures 12 and 13 show the drive-stage performance that was obtained from this testing. As previously mentioned, the drive stage can supply the base drive needed for a peak current output for a wide range of drive supply voltage. The curve in figure 12 shows that the drive circuit is capable of supplying sufficient base drive to maintain a 200-ampere

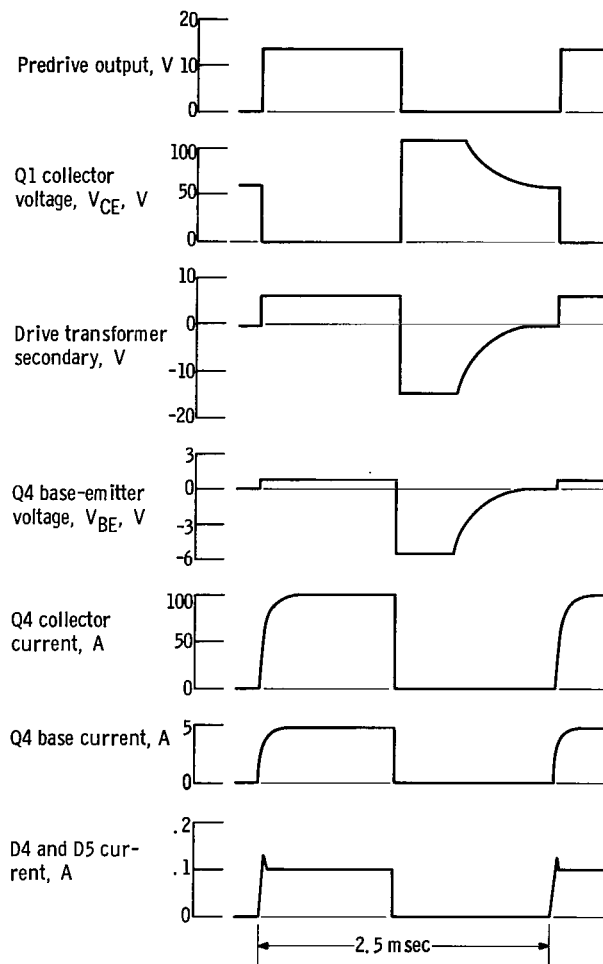


Figure 11. - Power circuitry waveforms.

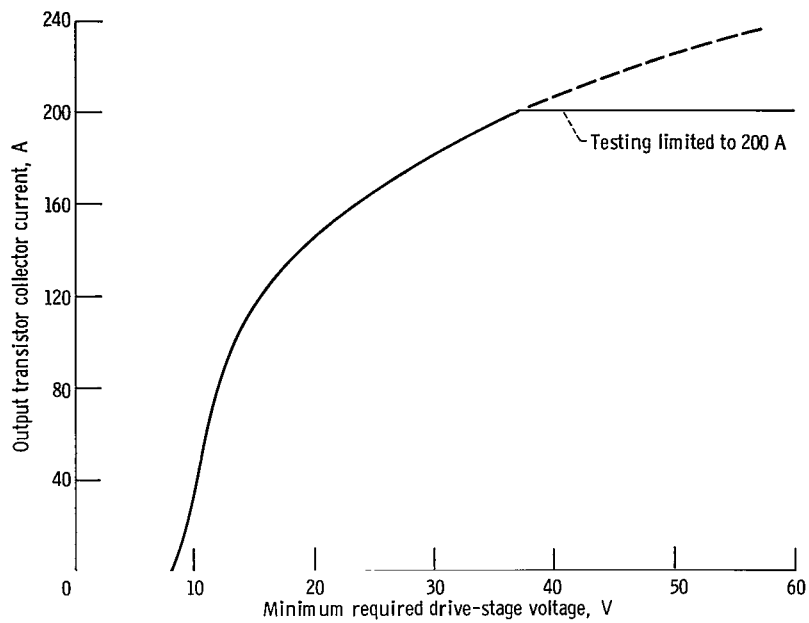


Figure 12. - Drive-stage capability.

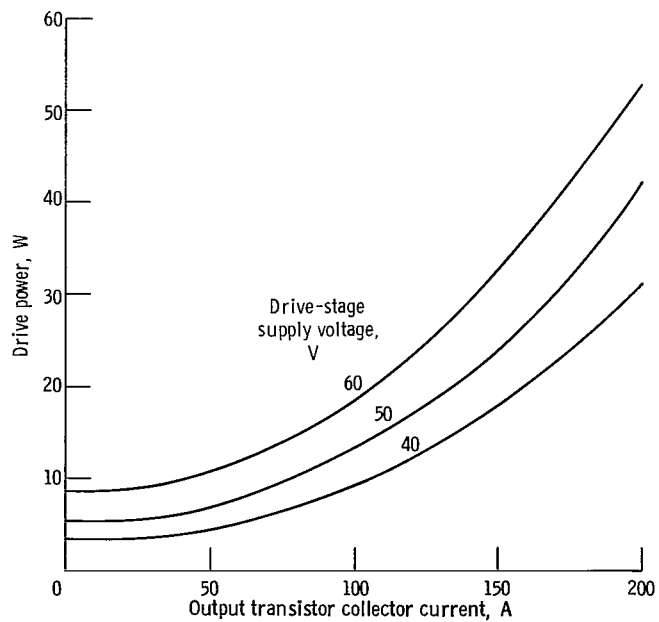


Figure 13. - Drive-stage power dissipation.

output transistor collector current for a drive supply voltage from less than 40 volts to 60 volts. Even with a 15-volt supply, the drive circuit can furnish enough base drive for over a 100-ampere output transistor collector current.

The curves in figure 13 show the drive-stage power dissipated as a function of output-stage transistor collector current for different drive-stage supply voltages. The magnetizing current loss and the loss in the current source resistor, R3, account for the fact that the curves are initially flat and do not go through zero. If these initial losses are disregarded for a given collector current, the power dissipation is approximately proportional to the drive supply voltage. For a standard base drive circuit using a series current-limiting resistor, the power dissipation would increase as the square of the drive supply voltage. Thus, the saturation sensing drive circuit used in this inverter greatly reduces power losses when operating over a range of drive supply voltage or output current.

Output stage. - The output stage of the inverter consists of three identical circuits, one for each phase. Each of these circuits uses two power transistors connected in a half-bridge configuration as shown in figure 14. The electrical load, in this case the alternator, is connected to the output stage through a contactor. Diodes D1 and D2 provide a path for reactive load currents to flow back to the supply. The complementary base drive signals for Q1 and Q2 are furnished by the drive-stage circuitry.

The half-bridge circuit provides ac power to the load by alternately connecting either side of the power supply to the load through the alternate conduction of Q1 and Q2. Any overlap in the conduction of Q1 and Q2 would result in a short across the power supply, causing high currents in Q1 and Q2. Since the typical turn-off time for an output transistor is about 15 microseconds at rated collector current, an overlap in conduction would occur unless there were a delay between base drive signals. As previously mentioned, the dwell-time circuitry solves this problem by delaying the leading edge of each base drive signal by approximately 100 microseconds. This time delay is to assure that the previously conducting transistor is turned off before the other transistor in the half-

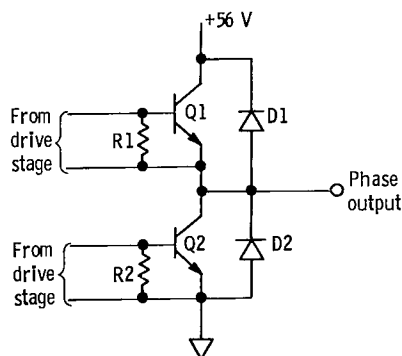


Figure 14. - Single-phase output stage.

bridge output stage starts conducting. Since reactive load current will be flowing in D1 or D2 during the 100-microsecond dwell time, the dwell time will not affect the output wave shape.

Input filter. - The input filter is necessary to attenuate the high third harmonic current that is present due to the alternator neutral being connected to the center tap of the dc source. This filter, shown in figure 15, consists of the mutual inductor L1 and capacitors C1 and C2. By using a mutual inductor on the dc buses, the magnetic core of the

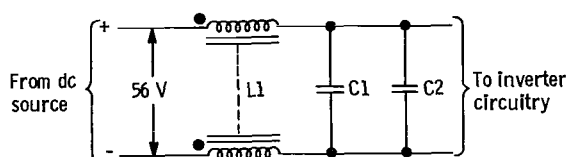


Figure 15. - Input filter.

inductor need only be sized for the current unbalance between the buses. This unbalance flows in the alternator neutral. Although the mutual inductor requires much less core area than two separate inductors and effectively attenuates the third harmonic neutral current, it is not effective in attenuating the ripple voltage caused by transistor switching. Capacitors C1 and C2 each consist of several capacitors paralleled together to obtain the desired capacitance value and to divide the ripple current among the capacitors. Capacitor C1 consists of ten 660-microfarad capacitors to perform most of the filtering. Capacitor C2 consists of seven 5-microfarad capacitors that have a small internal series resistance and are more effective for attenuating higher frequencies.

BRAYTON SYSTEM STARTUP USING THE MOTOR-START INVERTER

A simplified schematic showing the use of the motor-start inverter in the Brayton system is shown in figure 16. The ± 28 -volt system battery supply provides the 56-volt input to the inverter. A contactor is used between the inverter and the alternator, so that the inverter is connected to the alternator only during the motoring period. Since the alternator neutral is always connected to the central tap of the dc source (system ground), circulating third harmonic currents are allowed to flow. If the alternator neutral were not connected during motoring, the inverter would not require the large input filter stage.

Approximately 50 system startups were made using the motor-start inverter. A typical system startup occurs in the following manner: The system heat source is brought up to temperature; the alternator load contactor is opened; the voltage regulator for the alternator is inhibited; and the alternator series field is shorted. Then, the inverter input contactor is closed; the contactor on the inverter output is closed; and the

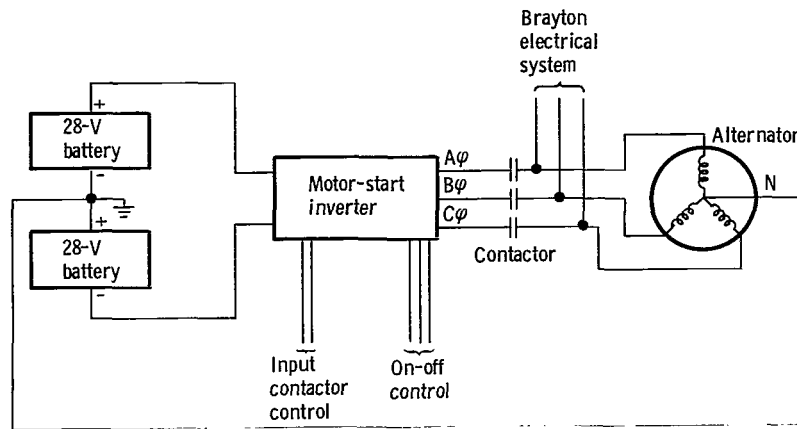


Figure 16. - Motor-start inverter connected to Brayton system.

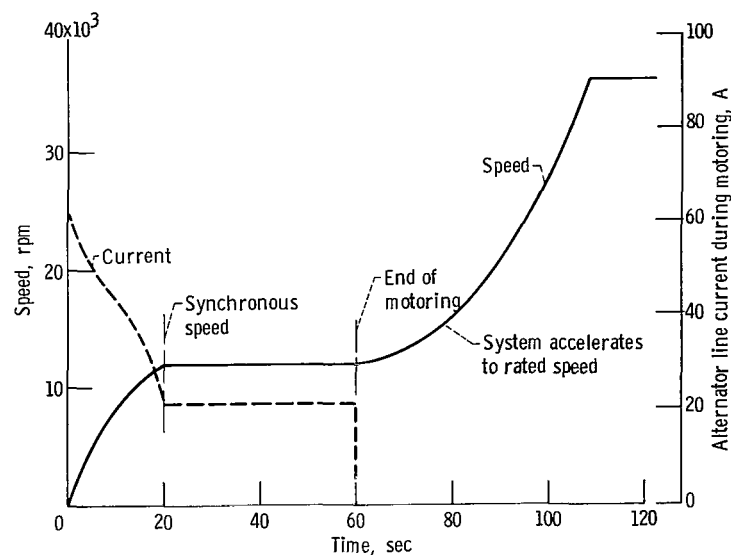


Figure 17. - Typical Brayton system startup using motor-start inverter.

inverter is pulsed on. System startup then occurs as shown in figure 17. For this startup it takes 20 seconds for the alternator to reach synchronous speed (12 000 rpm). The required current falls rapidly as the speed increases from zero to synchronous speed. During the motoring period, the gas in the power loop of the Brayton system is circulated, increasing its temperature. At the end of 1 minute the inverter is shut off and the system is allowed to bootstrap itself up to rated speed (36 000 rpm). During this time, the inverter is isolated from the system by opening the contactors on the inverter input and output; the short is removed from the series field; and the voltage regulator inhibit is removed. As the system approaches rated speed, the speed control assumes regulation of system speed.

CONCLUDING REMARKS

A three-phase, 400-hertz, 15-kilovolt-ampere prototype static inverter was designed and fabricated to motor-start the isotope Brayton space power system. This inverter was successfully used for 50 Brayton system startups. Motor starting, by eliminating the need for gas-injection starting, may permit significant reduction in both the complexity and weight of the gas-management system.

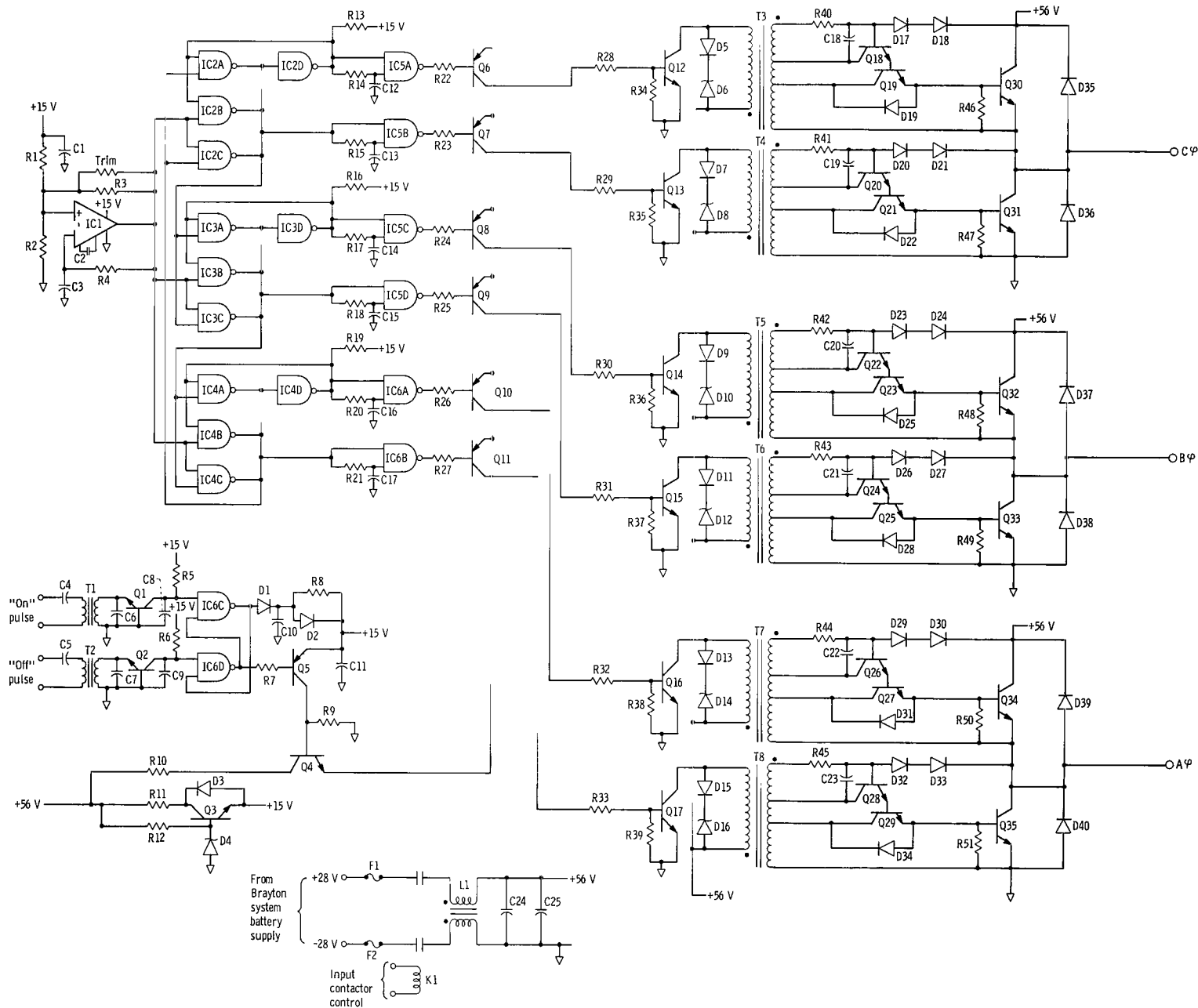
The major inverter requirement is the ability to supply a large peak starting current to the Brayton alternator for a short period of time. The remainder of the inverter operation is a lower power motoring condition at near synchronous speed. Previous Brayton system testing demonstrated that a 400-hertz, 20-volt, rms, line-to-neutral voltage motoring condition would produce self-sustaining system operation. The inverter was therefore designed to produce a 400-hertz, 28-volt, rms output, allowing the inverter to operate directly from the 56-volt dc system bus, eliminating the need for an output transformer or input voltage converter stage. The inverter has a 200-ampere peak current rating. For design simplicity, a quasi-square-wave output was chosen.

Linear and digital integrated circuitry is used to generate the three-phase, 400-hertz reference signals. A saturation sensing drive stage is used to improve switching speed and to provide efficient operation over a range of output current and drive supply voltage, eliminating the need for a regulated drive-stage supply regulator. A pulse-operated on-off control circuit is provided to interface with the Brayton system controls. An input contactor is included in the design so that the inverter is isolated from the system dc bus when not in use.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, November 9, 1971,
112-27.

APPENDIX - COMPLETE INVERTER SCHEMATIC DIAGRAM AND PARTS LIST

Reference designation	Part number	Description
D1, D2	1N914	75 mA, 75 V, fast recovery
D3, D5, D7, D9	1N4942	1 A, 200 V
D11, D13, D15, D17 to D34		
D4	1N3025	1 W, 16 V, zener
D6, D8, D10, D12, D14, D16	1N3000B	10 W, 62 V, zener
D35 to D40	1N1186	35 A, 200 V
C1, C4 to C7		0.1 μ F, 50 V
C2		10 pF, 50 V
C3		0.047 μ F, 400 V
C8, C9		510 pF, 100 V
C18 to C23		0.005 μ F, 1000 V
C10, C11		8.2 μ F, 20 V
C12 to C17		0.01 μ F, 50 V
C24		ten 660- μ F, 85-V tantalum capacitors in parallel
C25		seven 5- μ F, 150-V metalized paper capacitors in parallel
IC1	μ A748	operational amplifier
IC2 to IC6	MC668L	quad, dual input NAND gate
L1		1:1 (seven turns on A1-47 core with 0.02-cm (8-mil) gap)
Q1, Q2	2N930	30 mA, 45 V
Q3, Q4	2N1724	5 A, 80 V
Q5 to Q11	2N2905A	600 mA, 60 V
Q12 to Q17	SDT-7152 (Solitron)	10 A, 200 V
Q18, Q20, Q22, Q24, Q26, Q29	1718-0602 (Westinghouse)	10 A, 60 V
Q19, Q21, Q23, Q25, Q27, Q29	1768-0630 (Westinghouse)	40 A, 60 V
Q30 to Q35	1401-1020 (Westinghouse)	250 A, 100 V
R1, R2, R14, R15, R17, R18, R20, R21		22 k Ω , 0.25 W
R3		16 k Ω , 0.25 W
R4, R7		10 k Ω , 0.25 W
R5, R6		47 k Ω , 0.25 W
R8		100 k Ω , 0.25 W
R9		4.7 k Ω , 0.25 W
R10		20 Ω , 25 W
R11		100 Ω , 2 W
R12		4.7 k Ω , 1 W
R13, R16, R19		8.2 k Ω , 0.25 W
R22 to R27		1.5 k Ω , 0.25 W
R28 to R33		50 Ω , 5 W
R34 to R39		100 Ω , 0.25 W
R40 to R45		30 Ω , 5 W
T1, T2		pulse transformer 200:80 (51402-1D core)
T3 to T8		drive transformer 252:13:14:25 (AH 129 core with a 0.02-cm (8-mil) gap)
K1		input contactor
F1, F2		100-A fuse



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